Program/Erase Characteristics of Amorphous Gallium Indium Zinc Oxide Nonvolatile Memory

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***Abstract*—Currently, both high-density 3-D stacking nonvolatile (NV) memory and embedded NV memory in advanced systems on panel (SOPs) urgently demand the assistance of new and functional transition metal–oxide materials. This is to overcome serious fabrication issues encountered in the use of conventional Si or poly-crystalline Si materials, as well as to increase storage density with lower process cost. This paper reports the fully functional NV memory structure operated by an ionic amorphous oxide semiconductor with a wide energy band gap (> 3.0 eV) in a Ga_2O_3-In_2O_3-ZnO (GIZO) system under low process temperature ($< 400\ ^\circ$C) while being combined with various metal–oxide materials of Al_2O_3, GIZO, and Al_2O_3 as the electron charge's tunneling, storage, and blocking layers, respectively. The different methods of memory programs and, especially, the unique erase characteristics caused by a much wider band gap than Si were intensively being investigated, and as a result, excellent electrical results of a large program/erase window over 3.8 V at a pulse time of 10 ms are achieved.**

***Index Terms*—Amorphous, gallium indium zinc oxide (GIZO), memory, nonvolatile (NV), oxide, program/erase (P/E), thin-film transistor (TFT).**

I. Introduction

CURRENTLY, new types of functional transition metal–oxide materials are attracting great interest in new types of memory device technologies [1]–[3]. This is because of the material advantages over the usual applied silicon (Si) or other conventional materials in terms of fundamental innovations to the conventional fabrication method, subsequently enhancing electronic products' performance and increasing circuit density. Meanwhile, as the device dimension scale into the nanoscale range, physical and electrical characteristics, as well as the reliability scaling challenges of the nonvolatile (NV) memory, become more serious [4]. A series of new technologies, such as the high-k material in storage cells and 3-D device structures and the low-k material for adjacent cell filling, has been developed to overcome those issues. On the other hand, layer-by-layer stacking devices on one substrate under low process temperature are considered as one of the most effective solutions to fundamentally relax these limits. Some types of multilayer resistive RAMs that are composed of transition metal–oxides, such as NiO or SrTiO3, and [$Pr_{1-x}Ca_xMnO_3$, (Praseodymium-Calcium-Manganese-Oxide)] [5]–[7] resistors and diodes have been explored for next-generation NV memory. Additionally, the two-layer NAND Flash memory by a highly stackable polycrystalline Si thin-film transistor (TFT) prototype has been presented [8]. However, most of these materials are expected to show diverse material and device characteristics between the intra- and intergrain due to the mixed-crystal structures. Therefore, it always results in nonuniform threshold voltage distribution in the electrical devices [9], which makes it difficult to apply them to mature electronic products, especially with the stringent uniformity requirement in the modern electronic industry.

One of the new transition metal–oxide materials, the ionic amorphous oxide semiconductor (IAOS) with a wide energy band gap (> 3.0 eV) in a Ga_2O_3-In_2O_3-ZnO system has been developed for future advanced transparent-display or flexible-display applications [10], [11]. This material, namely, amorphous gallium indium zinc oxide (a-GIZO), demonstrates an electron mobility that is one magnitude higher ($\geq 10\ \mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$) than that of a-Si:H, even with a similar amorphous state, which is attributed to the different material structure and electron conduction mechanics. A number of applications, even with the simple inverter or oscillator circuit based on this material [12]–[14] for the value-added application in the system on panel (SOP), have been explored. For a long time, to support the most advanced SOP product incorporating the CPU and memory circuit, low-temperature poly-crystalline TFTs by various advanced crystallization methods have extensively been developed [15], [16]. However, these techniques always suffer the similar issue of nonuniform electrical characteristics in 3-D stacking memory.

In this paper, for the first time, the material structure and electrical characteristics of an a-GIZO TFT with a fully functional NV memory structure for applications of 3-D stacking memory or embedded memory in advanced SOP are demonstrated. The memory electrical characteristics, especially for the unique memory erase characteristics due to the special charge injection mechanics for the standard memory structure on a special wide-gap oxide semiconductor, were intensively investigated, and finally, a good program/erase (P/E) window and speed were achieved.

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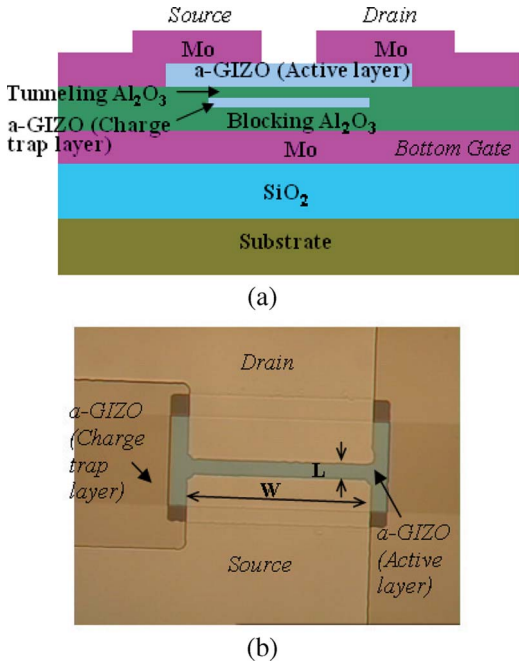

Fig. 1. (a) Cross-sectional view and (b) top view of the wide-band-gap a-GIZO TFT NV memory using the a-GIZO and Al_2O_3 as charge trap layer and gate insulators, respectively.

II. Fabrication Process

The schematic cross-sectional structure of an a-GIZO TFT with an NV memory structure is shown in Fig. 1, where the top-view optical image by microscope is also included. The device has an inverted staggered bottom-gate structure. At first, a 100-nm metal Mo for the bottom-gate electrode was deposited by magnetic RF sputtering on a 6-in Si wafer covered with 500-nm-thick oxide. The sandwich charge storage structure consisted of three layers of 35-nm atom-layer-deposition (ALD) aluminum oxide (Al_2O_3), 20-nm a-GIZO, and 10-nm ALD Al_2O_3, which were formed with the following steps for NV memory application. In this structure, the a-GIZO was deposited by magnetic RF sputtering at room temperature and formed with the floating-gate-type pattern by a standard lithograph and wet etch (diluted hydrofluoric acid) process before the second time deposition of the Al_2O_3. Later, another 70-nm-thick a-GIZO is deposited by sputtering and formed by a similar lithograph and etch process for the TFT active layer before the final formation of source/drain (S/D) electrodes by Mo. The highest temperature during this process was less than 400 °C.

During the a-GIZO sputtering process, the target of GIZO (Ga_2O_3 : In_2O_3 : ZnO = 1:1:1, or Ga : In : Zn = 2:2:1) with the source gas $Ar/O_2 = 19/1$ is applied to keep the electron concentration below 5×10^{19} cm^{-3} [10], [11] to form an appropriate semiconducting material. A number of other amorphous ionic oxides, such as a-IZO or a-IO, have higher carrier mobility; however, it is very difficult to keep the electron carrier concentration below 1×10^{20} cm^{-3} and be more like a conductor, and the devices with these materials show very high leakage.

The deposited a-GIZO shows a homogeneous amorphous state confirmed by the X-ray diffraction data presented in a previous publication [17]. Even as the process temperature increases to 600 °C, the film has no clear sharp peak observed and has, in fact, kept its amorphous state. The cross-sectional view of the transmission electron microscopy (TEM) image, high-resolution TEM (HRTEM) image, and secondary ion mass spectrometry (SIMS) depth profile analysis data is shown in Fig. 2(a)–(c), which demonstrates detailed information of the materials and the device structure. The HRTEM image of the charge trapping and active layer with a larger image resolution indicates that the GIZO layers still keep their amorphous states after a series of device fabrication steps.

III. Result and Discussion

Fig. 3 shows the representative drain-current/gate-voltage (I_{ds}–V_{gs}) transfer characteristics of an n-type a-GIZO TFT with an NV memory structure under $V_{ds} = 0.1$ V and 1.1 V without any postannealing. (Normally, a 1-h annealing in a 350 °C furnace with pure N_2 is necessary.) The geometric size of all devices studied in this paper is fixed with a channel width/channel length of $(W/L) = 50/4$ μm. In this figure, the TFT's threshold voltage V_{th} is defined as the gate voltage inducing a drain current equal to $W \times 1$ nA/μm and equal to 0.7 V at $V_{ds} = 1.1$ V. The saturation current is 0.52 μA/μm at $V_{ds} = 0.1$ V, and the estimated electron carrier field-effect mobility μ_{FE} calculated by the traditional one-order approximation definition equation [18] is 10.3 $cm^2/V \cdot s$. Moreover, the on–off current ratio I_{ON}/I_{OFF} is greater than 5×10^6, and the subthreshold slope is 207 mV/dec. The measured direct current performance merits are much better than those of a-Si:H TFT and are able to arrive at the basic device requirement for operating circuits in an SOP.

The typical programmed and erased I_{ds}–V_{gs} curves of the a-GIZO TFT NV memory without postannealing are shown in Fig. 4. In this figure, clear positive and negative shiftings of the I_{ds}–V_{gs} curves due to the channel hot electron (CHE) program mode ($V_{gs} = +12$ V, $V_{ds} = +8$ or 9 V) and one kind of band-to-band tunneling-induced hot hole injection (BB-HHI) erase modes ($V_{gs} = +12$ V, $V_{ds} = +10$ or 11 V) are observed, respectively [19], [20]. The detailed mechanics of these program and special erase behaviors will be discussed later.

Except for the CHE/BB-HHI program, the direct +F-N mode ($V_{gs} > 0$ V) and −F-N mode ($V_{gs} < 0$ V) on this structure are also investigated while the S/D are grounded. The measured results, together with the comparisons of CHE/BB-HHI, are summarized in Fig. 5, which employ the shifted threshold voltages (ΔV_{th}) to qualify the specific P/E characteristics of the devices under different bias conditions. In this figure, +F-N properly programs the device like CHE. At a time of 10 ms, the device with both +F-N and CHE modes achieved program window $\Delta V_{th} > 4.0$ V. However, −F-N, which is normally used for an erasing device, provokes very small negative ΔV_{th} in the a-GIZO TFT NV memory. With $V_{gs} = -14$ V at time = 10 ms, V_{th} shifted by only −0.50 V is observed, which is much less than the positively shifted V_{th} under counterpart program conditions.

The possible reason for this phenomena is that a-GIZO is a natural n-type semiconductor following the ionic oxide

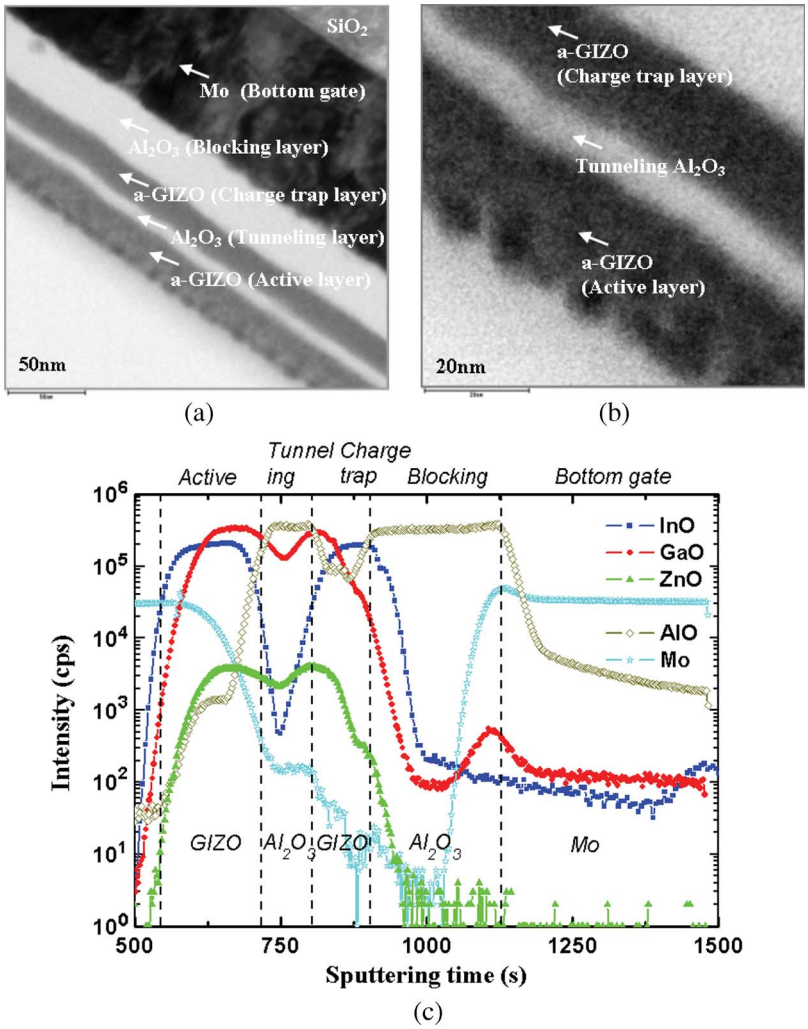

Fig. 2. (a) TEM image, (b) HRTEM image, and (c) SIMS depth profile analysis data of the a-GIZO TFT NV memory using 10-nm Al_2O_3, 20-nm a-GIZO, and 35-nm Al_2O_3 as the charge tunneling layer, trap layer, and blocking layer, respectively.

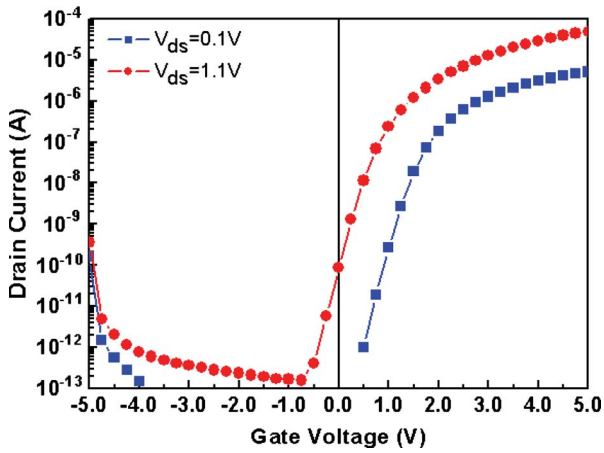

Fig. 3. TFT transfer characteristics of the a-GIZO TFT NV memory before postannealing with channel width/channel length $W/L = 50/4\ \mu$m.

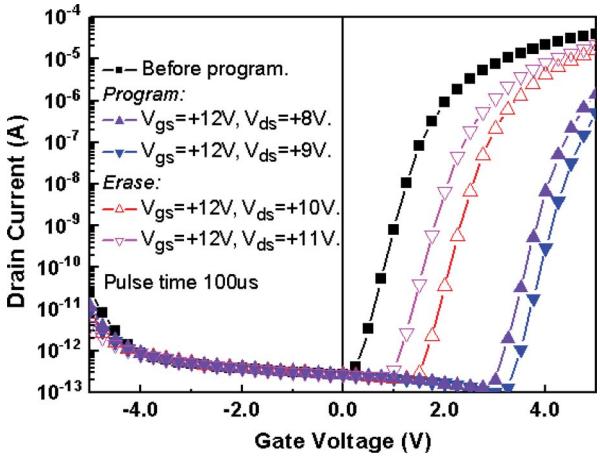

Fig. 4. Typical programmed and erased I_{ds}–V_{gs} curves of the a-GIZO TFT NV memory under different stressing conditions.

semiconductor conductance mechanics [11], which is much different from the silicon that is easily doped by *V*- or *III*-column ions and turns into an n-type or a p-type semiconductor, respectively. For a-GIZO, there are only electrons that move around the outmost s-orbital of the neighboring indium or zinc cations and induce the n-type carriers in the device channel to take in the charge transfer through the conduction band minimum in the energy band gap. Since there is no effective

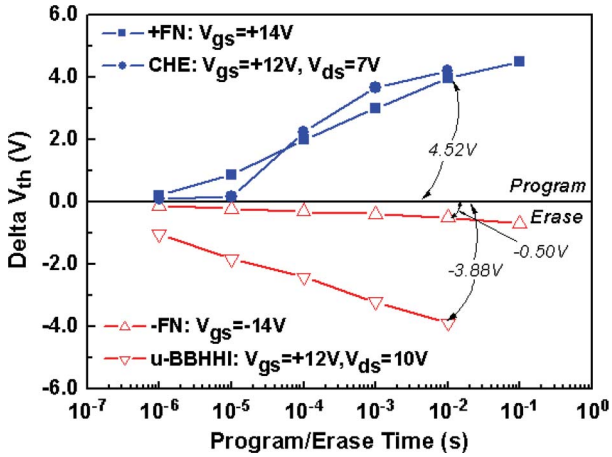

Fig. 5. Summary of the a-GIZO TFT NV memory P/E results by different methods.

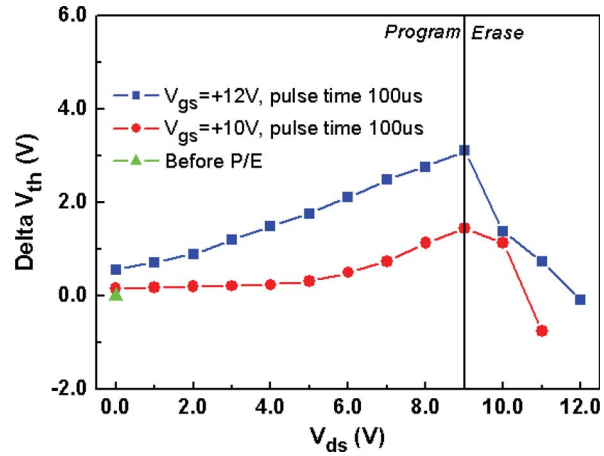

Fig. 6. Shifted $V_{\rm th}$ (programmed $V_{\rm th}$–fresh $V_{\rm th}$) as a function of different $V_{\rm ds}$'s in the a-GIZO TFT NV memory.

conductance method available for majority electrons in a-GIZO moving in one direction under an externally applied electrical field, which induces the p-type carriers in the device channel to take in the positive charges at a relatively low-energy-level valance band maximum, the hole carrier is difficult to be achieved in all IAOS [11]. Due to this fact, very few holes are available for device erasing when the gate is negatively biased, and a very small negative $\Delta V_{\rm th}$ under $-$F-N was observed. In contrast, a large positive $\Delta V_{\rm th}$ is still available through a proper program method with electron injection. As a result, this is one of the disadvantages of the a-GIZO TFT NV memory compared with the conventional Si MOSFET NV memory, which constantly demonstrates similar positive and negative $\Delta V_{\rm th}$ under the $+$F-N and $-$F-N modes, respectively.

Nevertheless, in Fig. 5, it needs to point out that the erase window by the HHI mode is much larger than that by $-$F-N and nearly symmetrical to the counterpart program window by CHE. With $V_{\rm gs} = +12$ V and $V_{\rm ds} = +10$ V at time $= 10$ ms, a -3.88-V $\Delta V_{\rm th}$ is observed. Here, the difference between the HHI erase and $-$F-N methods is whether the drain voltage is applied. Therefore, the drain voltage effect on the memory erase characteristic is particularly investigated and shown in Fig. 6. While $V_{\rm gs}$ is fixed and $V_{\rm ds}$ is increased up to 10 V, the device

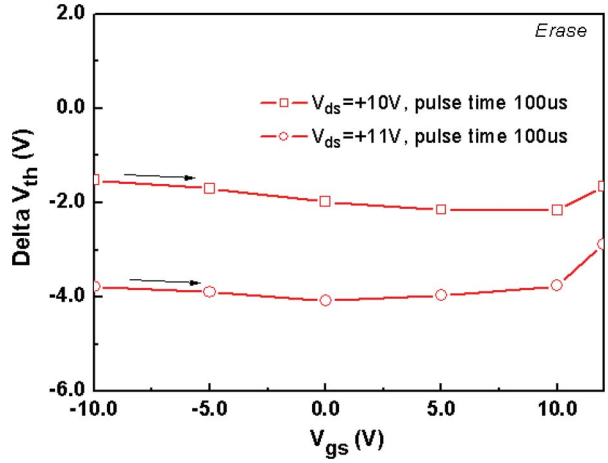

Fig. 7. Erased $\Delta V_{\rm th}$ as a function of different $V_{\rm gs}$'s in the a-GIZO TFT NV memory.

shows normal CHE program characteristics, with $V_{\rm th}$ positively shifting and the programmed window increasing well. However, once $V_{\rm ds}$ is greater than 10 V, $V_{\rm th}$ abruptly becomes negatively shifting and shows an erasing behavior. Furthermore, in Fig. 7, as the gate voltage is altered from -10 V to $+12$ V, the negatively shifted $V_{\rm th}$ almost stays at the same value level, whereas the drain voltage is set at 10 or 11 V for erasing the a-GIZO TFT NV memory. It means that, regardless of the polarity and magnitude of the gate voltage, erasing an a-GIZO TFT NV memory mainly depends on the level of drain voltage. It is different from the erasing characteristics of a Si MOSFET NV memory with a similar BB-HHI erase mode, which always needs $V_{\rm gs} < 0$ and $V_{\rm ds} > |V_{\rm gs}| > 0$ to attain the correct erasing characteristics.

These special erasing characteristics of the a-GIZO NV memory are thought to be the effect of one kind of avalanche BB-HHI stressing on a unique structure with wide material energy band. Similar to the n-type Si MOSFET NV memory, the large positive drain voltage lets the drain n-p junction to become reversely biased. While the energy band bending in the junction depletion region is higher than the semiconductor band gap, the direct tunneling of electrons from the conduct band minimum in the n-type semiconductor to the valence band maximum (VBM) in the p-type semiconductor becomes significant, and holes are then left on the VBM. Then, most electrons are collected by the drain terminal voltage, and some lucky holes get enough energy under the negative gate voltage to overcome the energy barrier limit between the channel and the tunneling insulator and to inject it into the charge trap layer. This neutralizes the trapped electrons in order to erase the programmed device. The huge tunneling electrical field is necessary for erasing the n-type Si MOSFET NV memory since the energy barrier of the hole-tunneling thin SiO_2 layer from the p-type Si for charging the trap layer is 4.2 eV. The energy band structures of the a-GIZO (channel)/Al_2O_3 (tunneling)/a-GIZO (trapping)/Al_2O_3 (blocking)/Mo (gate) system are depicted in Fig. 8(a). The energy barrier for an electron tunneling from the a-GIZO channel into the trapping layer is 3.0 eV, which is very close to the value of 3.15 eV for a normal Si/SiO_2 system. In contrast, this hole barrier is only 2.0 eV in

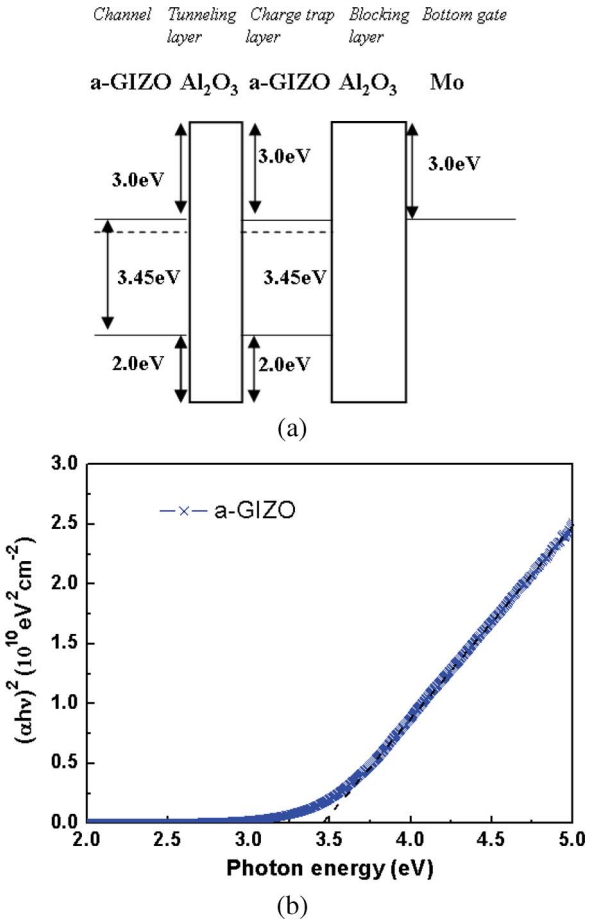

Fig. 8. Energy band structures of the a-GIZO (channel)/Al_2O_3 (tunneling)/a-GIZO (trapping)/Al_2O_3 (blocking)/Mo (gate) system. (a) Energy band distribution level. (b) a-GIZO band gap estimated from the function of $(\alpha hv)^2$ versus hv derive from the measured optical absorption coefficient α gathered by the UV-visible spectrophotometer.

the a-GIZO TFT NV memory, which is much less than that of the Si-SiO_2 system, because the a-GIZO has a wide-band-gap material with a value of approximately 3.45 eV. This band gap is estimated from the data gathered from the optical absorption coefficient α versus the wavelength plot by the UV-visible spectrophotometer in Fig. 8(b) [21].

In addition, unlike the homogeneous junction in Si MOSFET, the S/D contact with the channel in the a-GIZO TFT is considered as heterojunction, which is capable of being considered as the Schottky barrier diode or the ohmic contact [22] with different process conditions. As a result, the a-GIZO TFT can be treated as an n-type Schottky barrier transistor [23], because it shows similar transistor and diode I–V characteristics. Therefore, the abrupt junction interface between the metal and the a-GIZO helps the occurrence of the carrier's band-to-band tunneling under a relatively low voltage. Hence, once the applied voltage is increased to some level ($\sim$10 V), the electrons near junction tunneling into the drain electrode become depleted around the GIZO surface. The energy band of GIZO would gravely bend down to bring about hole accumulation around the surface for the charge balance. These holes are locally accelerated in the junction depletion region by a built-in electrical field or by the drain electrical field

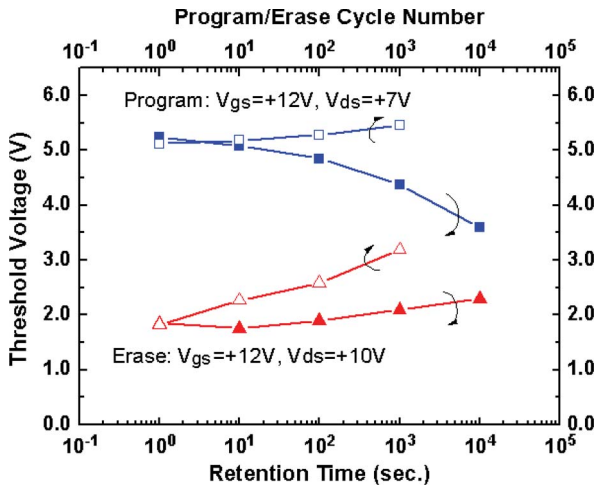

Fig. 9. P/E endurance and data retention characteristics of a-GIZO TFT NV memory.

since there is a long overlap length ($> 2\ \mu$m) between the drain electrode and the gate electrode. Subsequently, a number of holes are injected into the gate insulator due to the small tunneling barrier ($\sim$2.0 eV) for the holes previously mentioned. For the hole-tunneling probability to surpass the electron-tunneling probability, the electrons (net negative charge) trapped in the trap layer are neutralized by the injected hole (positive charge), and the device's $V_{\rm th}$ turns from positively shifting to negatively shifting. This speculation principally explained the unique erasing behavior of the a-GIZO NV memory decided by the drain voltage, regardless of the gate voltage. However, it needs quantitative work to confirm it in future.

The memory reliability characteristics, including P/E endurance and data retention characteristics, are shown in Fig. 9. In the figure, as the P/E cycles are greater than 10^3 times or the retention time is more than 10^3 s, the programmed window decreased to be below 2.5 V. The results indicate that the a-GIZO NV memory without postannealing does not have the same good reliability as a normal Si NV memory. The possible reason is believed to be that the a-GIZO film itself is sensitive to the atmosphere (especially, O_2) and becomes unstable under long time exposure to air or electrical field stressing [18], [24]. The trapped charge in the trap layer easily escapes due to the film variation or is neutralized by the charges in the gate insulator and gate-insulator/channel interface. In addition, the accumulation of these charges in the gate insulator and interface also degrades the P/E window after a number of cycles.

IV. Summary

We demonstrated the possibility of producing NV memory by using an a-GIZO TFT as the driver and an a-GIZO as the charge trap layer under low process temperature. The memory program and, especially, the erase characteristics for the unique material structure are extensively investigated. The excellent P/E characteristics of the P/E window $>$ 3.8 V at time $=$ 10 ms on these oxide devices indicate that this technology is expected to be a promising choice in advanced SOP or 3-D stacking Flash memory products for the uniform film, low process temperature, and simple process steps.

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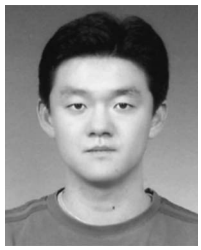

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