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Random Network Transistors of Carbon Nanotubes Directly Grown on Glass Substrate

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***Abstract*—We report a transistor of randomly networked single-walled carbon nanotubes (SWNTs) grown on glass by using water plasma CVD. The density of the nanotube on pre-patterned region was more than 50/μm^2 which is much larger than the percolation threshold. The nanotube network transistors were fabricated with Al_2O_3 for the gate oxide and a conducting and transparent ZnO for the back-gate. These nanotube active devices may be fitted to thin film transistor applications for future opto-electronics.**

Keywords-component; Thin Film Transistors, SWNT, Glass substrate, Conducting ZnO fims

I. Introduction

Carbon nanotubes (CNTs) have attracted much interest due to their unique physical properties and potential for diverse electronic device applications. The high room temperature mobility of semiconducting nanotubes gave special attention to field-effect transistors for microelectronic applications [1]. However, the fraction of metallic tube and precise position control of the individual nanotubes still require much work to apply carbon nanotubes for the active devices. Recently thin film transistors based on two-dimensional networks of carbon nanotubes were proposed to overcome or reduce such technical barriers [2]. The performance of this new transistor scheme was also evaluated with a computational model of heterogeneous percolating networks [3].

Nanotube network transistors, considering their dimensions, can be easily adopted for the display technology, for examples, thin film transistors (TFTs) in liquid crystal display (LCD) or organic light emitting diode (OLED). To obtain a flexible choice of the transparent substrates by overcoming high growth temperature of SWNTs, a spray method was introduced for a plastic substrate with a suspension of nanotubes. However, chemical vapor deposition (CVD) is the most compatible growth method for such applications, since nanotubes can be directly and selectively grown on substrates wherein catalyst are pre-patterned with iron, cobalt or nickel. The low strain temperature (~ 660 ^{o}C) of the best display glass is a crucial barrier to directly grow nanotubes on glass, since CVD of SWNTs generally requires higher growth temperature than 700 ^{o}C. Although several groups had tried nanotube growth on glass by thermal or plasma-enhanced CVD (PECVD), the grown nanotubes were multi-walled or they used highly expensive quartz glass. Recently, we demonstrated that SWNTs could be grown at 450 ^{o}C on SiO_2/Si substrates by remote plasma CVD system with water plasma [4,5]. Here we report the network transistors with SWNTs directly grown on glass.

II. Experiment

We used a Corning 1737 glass for substrate as shown in Fig. 1-(a), commercialized for the flat panel displays, which has high strain point of 660 ^{o}C. A conducting and transparent ZnO film (50 nm) deposited by atomic layer deposition (ALD) was used for the back-gate with a resistivity in the order of 10^{-3} Ωcm. A 200-nm-thick Al_2O_3 was also followed by ALD for a gate dielectric before the catalyst layer formation.

The SWNT network was formed on the pre-patterned catalyst regions between source and drain as shown in insert of Fig. 1(a) with a direct photolithographic technique using a simple mixture of ferrocene and conventional photoresist [6]. Nanotube growth was performed at 550 °C with a water plasma power of 15 W in a lamp-heating type radio frequency (rf, 13.56 MHz) remote PECVD system using CH_4 gas. Glass substrates were placed with a silicon wafer on quartz holder in the manner of glass/silicon/quartz holder to support absorption of white light from halogen lamp, and other growth conditions were similar to the previous report [4,5]. The transistors were completed with formation of the electrodes for source and drain with Ti (10 nm)/Au (100 nm) by standard lift-off method.

III. Results and Discusson

Fig. 1(b) shows grown nanotubes with 0.03 M of ferrocene concentration in photoresist. The grown nanotubes form a continuous SWNT film or 'SWNT mat' whose density is more than 50/μm^2 with 1~5μm of nanotube length. A schematic of the network transistor is shown in Figure 1(c). Raman spectra from 633 nm laser excitation in Fig. 2(a) reveal that the grown nanotubes were single-walled as characterized by the strong G-band (tangential stretch mode) and the presence of the sharp radial breathing mode (RBM) (see insert of Fig. 2(a)). The intensity ratio of D-band relative to G-band (I_D/I_G) can be used

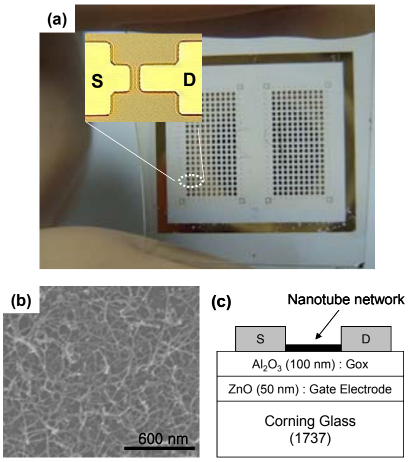

Figure 1. Thin film transistors fabricated on the transparent glass substrate. (a) Optical image of the transistor array on glass. Insert is a magnified TFT which is transparent except the electrodes for source and drain. (b) SEM image of SWNTs that builds an active channel. (c) A schematic of the TFT transistor with the SWNT mat

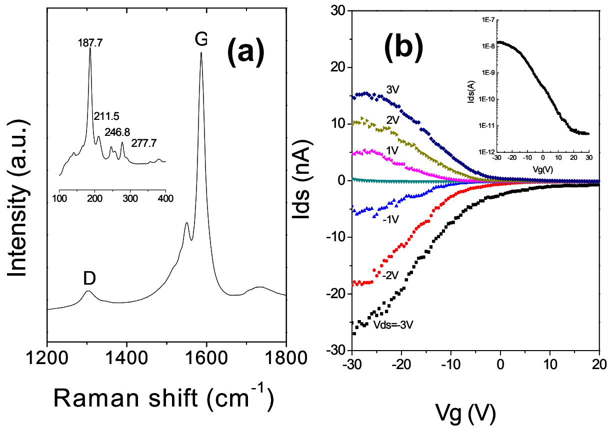

Figure 2. (a) Raman spectra (633 nm) for the SWNT mat shown in Fig.1(b) and the inset was enlarged RBM peaks. (b) The transistor characteristics for the network transistor with 10 μm of channel length and 50 μm of width. Insert indicates Log(I_{ds}) with V_{ds}=2 Volt

to evaluate the quality of the grown nanotubes. The I_D/I_G ratio (0.07) of the specimen shows fairy low value. The diameter (d_t, nm) of SWNTs can be calculated from the frequency (ω_{RBM}, cm^{-1}) of the RBM by the equation, $\omega_{RBM} = A/d_t, + B$ where A and B are experimentally found to be 223.5 cm^{-1}nm and 12.5 cm^{-1} for SWNTs. The corresponding diameters of the main peaks are 1.27, 0.95, 0.91, and 0.84 nm.

Fig. 2(b) shows the transistor characteristics for the network transistor with 10 μm of channel length and 50 μm of width. Insert indicates Log (I_{ds}) with V_{ds}=2 Volt. It exhibits an on-off ratio of ~ 10^4 with a subthreshold slop S ~ 10 Volt/decade. Ambipolar behavior from the gating of the Schottky barriers at the nanotube/Ti contacts reduces to a p-type semiconducting behavior which is attributed to suppress electron current with adsorption of oxygen molecules on nanotube surfaces in the ambient air [7]. The on-off switching in the transistor characteristics is attributed to heterogeneous percolating networks of metallic and semiconducting nanotubes. Snow et al. showed that a random network of nanotubes is electrically conducting above the percolation threshold of 0.3/μm^2 for nanotube density with its length of 1~3 μm [2]. However, even though the density of the nanotube mat is much higher than the percolation threshold, the network transistor shows typical *p*-type semiconducting characteristics with an on/off ratio of ~ 10^4 as shown in Figure 2(b). Li et al. reported that 90 % of the nanotubes grown by remote PECVD are semiconducting due to a thermodynamic factor [8].

The subthreshold slope of the nanotube field effect transistor is given by $(kT/q)\ln(10)[1-(C_{IT}/C_{ox})]$[3]. The capacitance, $C_{IT} = d(qN_{IT})/d(\phi_s)$, due to the total trapped hole charges (N_{IT}) at interface between nanotubes and gate oxide, and on nanotube surfaces, is estimated as about 160 times of C_{ox} (~0.3 pF/cm for 100 nm of Al_2O_3) for the subthreshold slop S ~ 10 Volt/decade. Our study shows that the large density of nanotubes in the SWNT mat intrinsically results in the poor subthreshold characteristic or low effective hole mobility with increase of the total trapped hole charges (N_{IT}). TFT application with the nanotube mat should reduce the trapped charges for better transistor performance. So we leave further studies for performance increase with the guides mentioned above.

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