Retention Reliability Improvement Using Nitride with Varying Trap Density in SONOS Type Non-volatile Memory

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Abstract

A new SONOS type structure employing bi-layered nitride with varying trap density and high-k blocking oxide is proposed for NAND Flash memory applications. The bi-layered silicon nitride with varying trap density is composed of a $SiN_x/Si3N_4$ stack and Al_2O_3 was used for the high-k blocking oxide. Compared with conventional SONOS structures, the proposed structure shows remarkable improvement of charge retention reliability while maintaining good programming/erase performance.

1. Introduction

Recently, there has been an increasing need of high density memory for mass storage applications such as memory cards, digital cameras, USB drives, etc. NAND Flash memory technology has been applied to these data storage application fields. With the continual scaling down of devices, however, conventional floating-gate based technology has limitations such as cell-to-cell coupling interference and disturbance in NAND Flash memory [1, 2]. Charge trapping memories, such as SONOS, are a promising solution to overcome the aforementioned floating-gate limitations. However, SONOS memory also has some problems for NAND Flash memory applications regarding high performance and reliability. One problem is that there is a strong trade-off between the programming/erase speed and charge retention in the conventional SONOS memory structure [3, 4].

In this paper, we propose a new SONOS type structure, where conventional silicon nitride and blocking oxide (SiO_2) are replaced with a bi-layered silicon nitride with varying trap density and a high-k blocking oxide (Al_2O_3), respectively, in order to mitigate the trade-off relationship between them. We fabricate both conventional and proposed devices and compare the electrical characteristics of these devices in terms of programming/erase speed and retention property.

2. Experimental

We fabricated MONOS and MHNOS type capacitor samples which are described in detail in Table 1. Both structures have different types of trapping nitride. One employs the uni-layered silicon-rich nitride (SiN_x). The other employs a bi-layered silicon nitride which consists of a SiN_x/Si_3N_4 stack. The stoichiometry of the Si_3N_4 layer is almost stoichiometric, as shown Table 2.

All samples were fabricated on p-type (100) wafers. The tunnel oxide was thermally grown at 850°C in an oxygen atmosphere and annealed in N_2O at the same temperature. Next, the uni-layered silicon nitride (SiNx) was formed using LPCVD at 730°C with a dichlorosilane (DCS)/NH_3 gas ratio of 2. In the case of bi-layered silicon nitride (SiN_x/Si_3N_4), the first nitride (Si_3N_4) was deposited using LPCVD at 730°C with a DCS/NH_3 gas ratio of 0.13 and the second nitride (SiN_x) was deposited using LPCVD at 730°C with a DCS/NH_3 gas ratio of 2.

For the bi-layered nitride, the first silicon nitride (Si_3N_4) layer on the tunnel oxide has a lower trap density while the second silicon nitride (SiN_x) has a relatively higher trap density, due to the higher DCS/NH_3 gas ratio [5]. Namely, the trap density varies within the bi-layered nitride structure.

Next, a blocking oxide (SiO_2) was also deposited using LPCVD at 450°C. In the case of high-k blocking oxide, Al_2O_3 was formed by atomic layer deposition (ALD) at 400°C using tri-methyl-aluminum (TMA) and ozone gas (O_3), followed by an O_2 anneal at 700°C for 1 min. Finally, after each dielectric stack was formed, Al or Pt electrodes were formed using conventional photolithography and evaporation processes.

MONOS type	MHNOS type
Tunnel oxide (SiO_2) 25 Å	Tunnel oxide (SiO_2) 30 Å
Trapping nitride 50 Å - SiN_x (50Å) - SiN_x (30Å) /Si_3N_4 (20Å)	Trapping nitride 60 Å - SiN_x (60Å) - SiN_x (40Å) /Si_3N_4 (20Å)
Blocking oxide (SiO_2) 70 Å	High-k Blocking oxide (Al_2O_3) 120 Å
Metal electrode (Al)	Metal electrode (Pt)

Table 1: Sample description of MONOS and MHNOS type devices.

	DCS/NH_3 ratio	Si (at %)	N (at %)	Stoichometry
SiNx	2/1	55.3	44.7	Si (3.9) N (3.1)
Si_3N_4	1/7.5	41.9	58.1	Si (2.95) N (4.05)

Table 2: Stoichiometry of Silicon nitride as DCS/NH3 gas ratio results from TEM EDS.

3. Result and Discussion

Generally, in SONOS type memories, Si-rich nitride (SiNx) with high trap densities results in improvement of programming speed with worse charge retention. Conversely, stoichiometric nitride (Si_3N_4) with low trap density leads to improvement in the charge retention, but has poor programming speed [5]. Trap density in the silicon nitride, as well as the thickness of tunnel oxide, is the main contributor to the trade-off

relationship between the programming/erase speed and the charge retention in SONOS devices. Therefore, we propose a SONOS type structure where the bi-layered nitride has varying trap density. The purpose of utilizing the bi-layered nitride is to improve the charge retention reliability while maintaining the programming/erase performance.

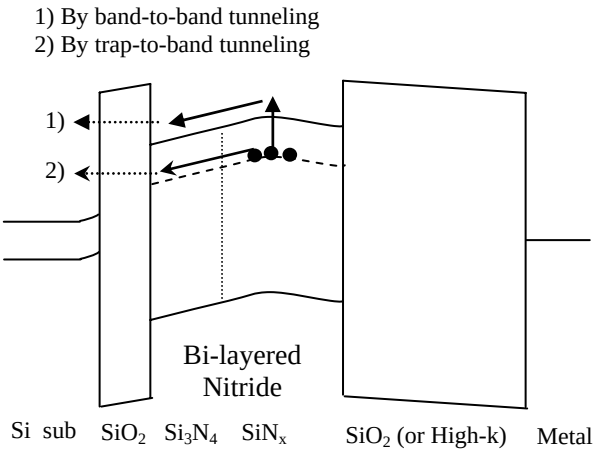

Fig. 1: Schematic band diagram illustrating the charge loss path in programmed state of MONOS or MHNOS structure with bi-layered nitride with varying trap density. Si_3N_4 has a low trap density and SiN_x has a high trap density

As shown in Fig.1, the charge loss paths in the programmed state energy band diagram of MONOS (or MHNOS) structure with bi-layered nitride are represented. A slight internal field exists in the structure due to the trapped charge distribution. With the two paths, the trapped charge can escape through the tunnel oxide to the substrate, whereas the blocking oxide is too physically thick for the trapped charge to leak through it. One path is leakage by band-to-band tunneling after Pool-Frenkel emission of the trapped charge. The other path is leakage by trap-to-band tunneling after transport of the trapped charge toward the trapping nitride-tunnel oxide interface. Leakage by trap-to-trap tunneling via traps in the tunnel oxide could also be included in the latter.

In the SONOS type structure with bi-layered nitride, leakage by trap-to-band tunneling after transport of the trapped charge toward the trapping nitride-tunnel oxide interface can be reduced, because transport of the trapped charge using a nitride trap as a stepping stone is reduced in the stoichiometric nitride (Si_3N_4) with low trap density. Lundkvist et al. also reported that the trapped charge tunnels from the nitride back to the silicon substrate due to the internal field in the retention mode and the charge loss rate is proportional to the trap density of the nitride [6].

The program/erase speed and programmed state retention characteristics of MONOS structure with uni-layered and bi-layered nitride are shown in Fig. 2 and Fig. 3, respectively. The charge retention characteristics are represented by the flat-band voltage shift due to the charge loss at the programmed state.

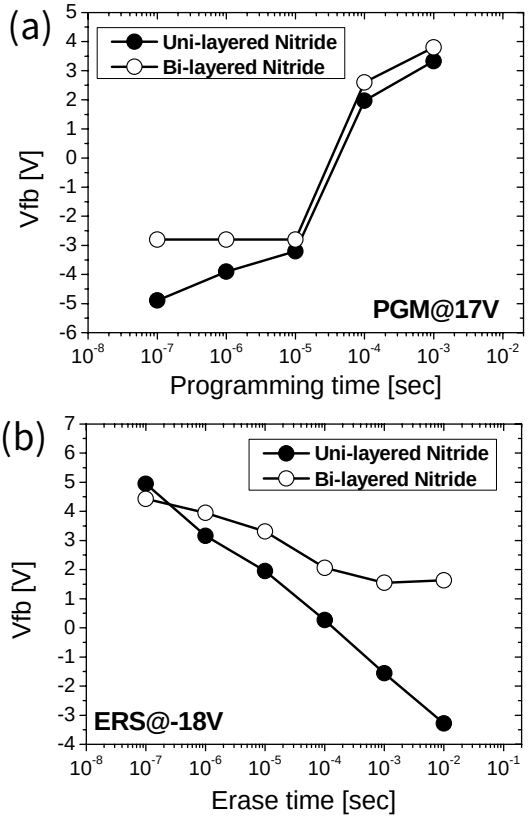

Fig. 2: (a) Programming and (b) erase characteristics of the MONOS device with uni-layered and bi-layered silicon nitride structure. Program and erase voltage are 17V and -18V, respectively.

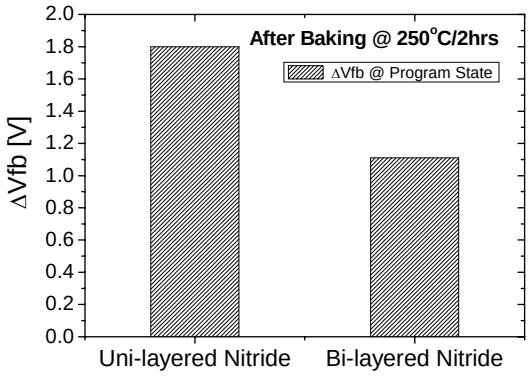

Fig. 3: Retention characteristics in the programmed state of the MONOS device with uni-layered and bi-layered silicon nitride structure. Flat-band voltage shift is measured after baking at 250 °C for 2 hours in the oven.

As expected, the retention characteristics of MONOS devices with bi-layered nitride are better than those with uni-layered nitride. Similar behavior is shown in the programming characteristics. However, in the case of the erase characteristics, MONOS devices with bi-layered nitride show worse performance. It could be thought that the stoichiometric silicon nitride with low trap density plays a role in reducing the amount of trapped charge tunneling back to the silicon substrate. The back-tunneling current from the gate also plays a

role for erase times over 100us. The trade-off relationship may still remain although it can be slightly improved with further thickness and process optimization of the structure.

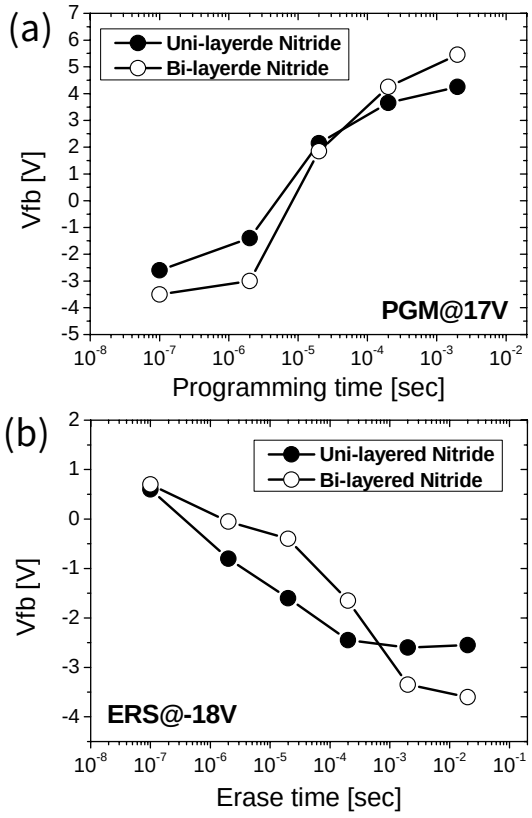

Fig. 4: (a) Programming and (b) erase characteristics of the MHNOS device with uni-layered and bi-layered silicon nitride structure. Program and erase voltage are 17V and -18V, respectively.

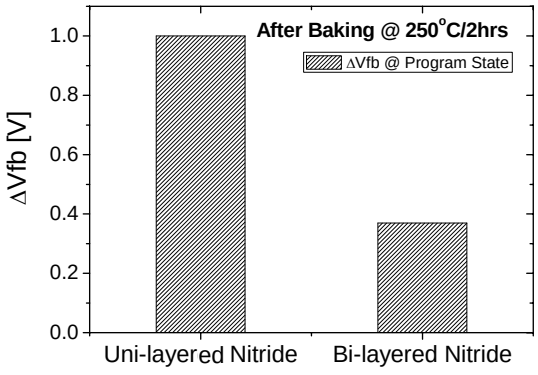

Fig. 5: Retention characteristics in the programmed state of the MHNOS device with uni-layered and bi-layered silicon nitride structure. Flat-band voltage shift is measured after baking at 250°C for 2 hours in the oven.

For this reason, high-k dielectric (Al_2O_3) was used for the blocking oxide in the MONOS structure with bi-layered nitride. By utilizing the high-k blocking oxide, the physical thickness can be increased without increasing EOT. Electric field in the tunnel oxide increases and the electric field in the blocking oxide decreases when the blocking oxide has a higher dielectric constant [7]. As a result, the back-tunneling current from the gate at the erase mode can be suppressed. In addition, the back-tunneling current from the gate can be further suppressed by utilizing high work-function metal gate such as Pt (≈5.3eV).

The programming/erase speed and the retention characteristics of MHNOS structure with uni-layered and bi-layered nitride are shown in Fig. 4 and Fig. 5, respectively. In the MHNOS device, the programming/erase characteristics are not deteriorated by utilizing bi-layered nitride in the structure. The programming/erase characteristics of the MHNOS device with bi-layered nitride is superior to those of the MHNOS device with uni-layered nitride for programming times longer than 30us and erase times longer than 500us. It is thought that the employment of the high-k blocking oxide and high work-function metal gate leads to the enhanced electric field in the tunnel oxide and the suppression of back-tunneling current from the gate. Thus, the negative effect of bi-layered nitride for the erase performance is reduced. For the retention characteristics, the effect of utilizing bi-layered nitride in the structure is remarkable. That is to say, the flat-band voltage shift by the charge loss is reduced to about 0.37V in the MHNOS device with bi-layered nitride.

4. Conclusion

We propose a new SONOS type structure with a bi-layered nitride layer with varying trap density and high-k blocking oxide. The results demonstrate that the charge retention reliability is remarkably improved while maintaining good program/erase performance for the proposed structure, compared with the conventional structure.

Acknowledgement

This work was supported by the National Program for Tera-Level Nano-Devices through the Ministry of Science and Technology, Korea.

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