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Large-scale assembly of 'type-switchable' field effect transistors based on carbon nanotubes and nanoparticles

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Abstract

We report the large-scale assembly of type-switchable field effect transistors (FETs) based on carbon nanotubes (CNTs) and nanoparticles (NPs). In this device, the charges stored in NPs adjacent to ambipolar CNT channels were adjusted to control the carrier type and density in the channels. We demonstrated the real-time reconfiguration of individual FET types and logic circuit functionality. Theoretical simulation of a model system was provided to explain this doping effect. This work takes advantage of the ambipolar properties of CNTs and opens up the possibility to build new types of devices with reconfigurable functionalities.

S Online supplementary data available from stacks.iop.org/Nano/21/345301/mmedia

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Efficient information processors such as a human brain are often based on the capability of reconfiguring individual circuits in real time. However, such capability has been extremely difficult to implement in conventional solid-state devices and often requires complicated circuits [1–17]. One fundamental limitation is the conventional doping strategy, where fixed dopant atoms permanently determine the device characteristics. For example, common silicon-based logic circuits are based on field effect transistors (FETs) whose charge carrier types are fixed as electrons (n-type) or holes (p-type) depending on dopant atoms. On the other hand, carbon-based nanostructures such as carbon nanotubes (CNTs) may have π-electrons as an intrinsic charge carrier without any dopant atoms. Furthermore, CNTs are known to contain both electrons and holes, indicating they can be operated as either n- or p-type channels depending on external fields. However, large-scale fabrication of type-switchable CNT-FETs, whose carrier types can be switchable in real time, has not been demonstrated before. Herein, we present the large-scale assembly method of 'type-switchable' FETs based on CNTs and nanoparticles (NPs), where the directed assembly strategy was combined with conventional microfabrication processes to fabricate the devices including CNT channels and adjacent nanoparticle-based charge storages. We adjusted the charges stored in the NPs adjacent to CNT channels to control the carrier type and density in the channels. Using this strategy, we could reconfigure the individual FET type and logic circuit functionality in real time. In addition, we provide theoretical simulations of a model system to explain this doping effect. In this work, we took advantage of the ambipolar properties of CNTs, opening up the possibility of new device architecture based on reconfigurable FETs.

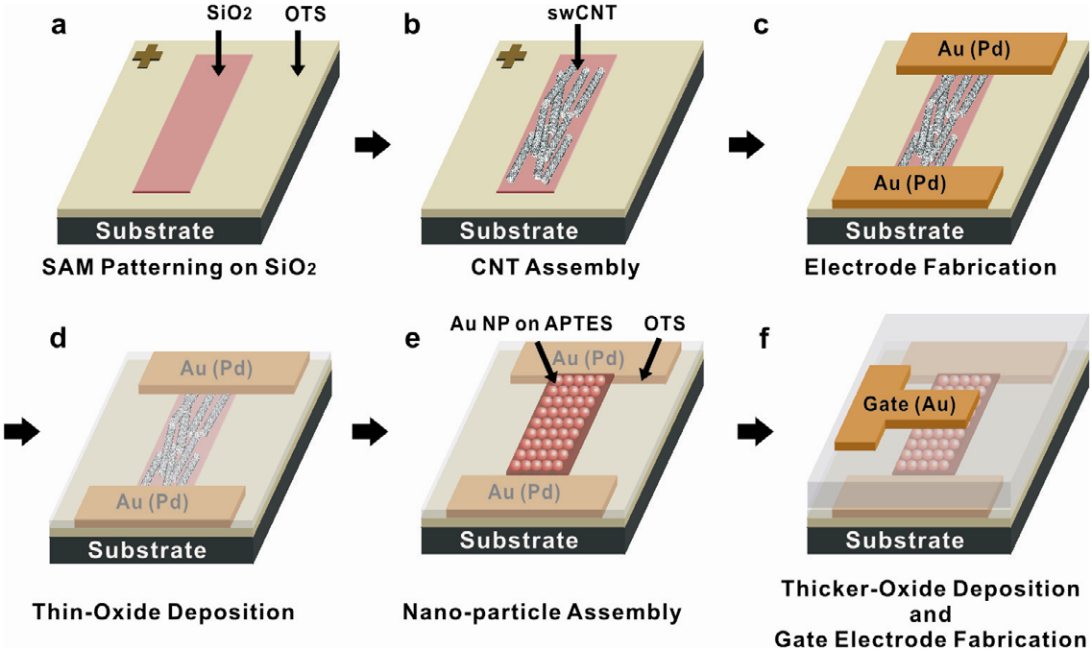

Figure 1. Fabrication process of type-switchable FETs based on CNTs and NPs.

2. Experimental methods

Our type-switchable FETs were fabricated by combining the assembly process of nanostructures with conventional microfabrication (figure 1 and experimental procedure in supporting information available at stacks.iop.org/Nano/21/345301/mmedia). First, a methyl-terminated self-assembled monolayer (SAM) such as octadecyltrichlorosilane (OTS) was patterned on SiO_2 film on highly doped silicon substrate (P-type) as reported before [18, 19]. The highly doped substrate below the SiO_2 film was used as a back-gate. When the substrate was placed in the single-walled CNT (swCNT) solution, swCNTs were assembled selectively on the bare SiO_2 regions [18, 19]. The source and drain electrodes were fabricated via the lift-off process. The selective breakdown of metallic swCNTs could be performed to achieve FETs with a high on–off ratio [20]. Then, a 1.5 nm-thick Al_2O_3 film was deposited via the atomic layer deposition (ALD) process using trimethylaluminum and water at 150 °C. The Al_2O_3 layer as high-k dielectric was advantageous as an insulating layer over the SiO_2 layer. In addition, the ALD process did not damage swCNTs unlike chemical vapor deposition of SiO_2. The OTS SAM and amine-terminated amino-propyltriethoxysilane (APTES) SAM were patterned on the Al_2O_3 film via photolithography [18, 19]. Here, APTES SAM was patterned on the Al_2O_3 surface over the swCNT channels. When the patterned substrate was placed in the Au NP solution, negatively charged Au NPs were assembled onto positively charged APTES SAM. After the NP assembly, a 50 nm-thick Al_2O_3 layer was deposited as gate insulator on the NP patterns. Finally, we fabricated top-gate electrodes on the Al_2O_3 layer. Noting that the entire fabrication process including the assembly of swCNTs and NPs was performed using conventional microfabrication equipment, our process is scalable for large-scale device fabrication and could be adapted by the current device industry for practical applications [18].

3. Result and discussion

3.1. Properties of type-switchable FETs

Figures 2(a) and (b) show the well-defined swCNT patterns (figure 1(c)) and NPs (figure 1(e)) between source and drain electrodes. The density of assembled NPs was about 20–25 μm^{-2}. Figure 2(c) shows multiple type-switchable FET devices over a large scale, confirming the mass production capability of our process. Note that the same process can be used to build nanoscale devices [21]. Interestingly, previous works show that the nanoscale devices fabricated by our method actually exhibited improved performance compared with macroscale ones, which has been explained by the effect of CNT alignment in the nanoscale channels [21]. Furthermore, one should be able to reduce the size of the charge storage layer by using smaller NPs, as reported previously [22].

When a large positive gate bias was applied, electrons tunnel from swCNTs to Au NPs through the thin Al_2O_3 layer. After removing the applied gate bias, the remaining negative charges in the NPs repelled electrons while attracting holes in the channels (left of figure 3(a)). Thus, the transistor exhibited p-type characteristics. Similarly, we achieved n-type channels by charging the NPs positively (right of figure 3(a)).

Figure 3(b) shows a typical hysteresis curve of our type-switchable FET. Here, the top-gate bias was swept with $\sim$0.36 V s^{-1} sweep speed under 1 V source–drain bias. Please note the crossing point (marked by a dotted circle), where the forward (from −10 to 10 V) or reverse (from 10 to −10 V) sweep curves exhibited a positive or negative slope indicating

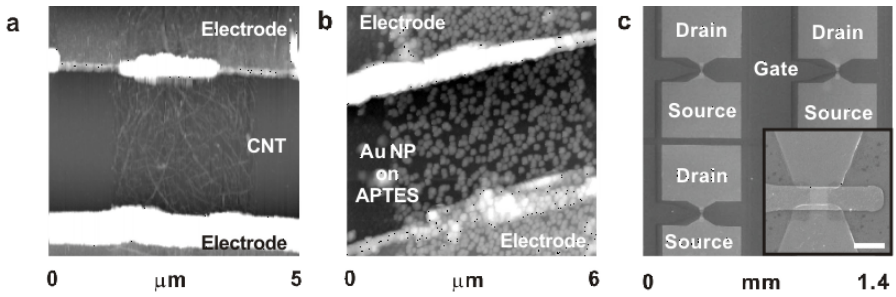

Figure 2. (a) Atomic force microscopy (AFM) topography of swCNT patterns between electrodes. (b) AFM topography of assembled Au NPs on the Al_2O_3 layer. (c) Scanning electron microscopy (SEM) image of type-switchable FETs over a large-scale area. The inset image shows a single type-switchable FET.

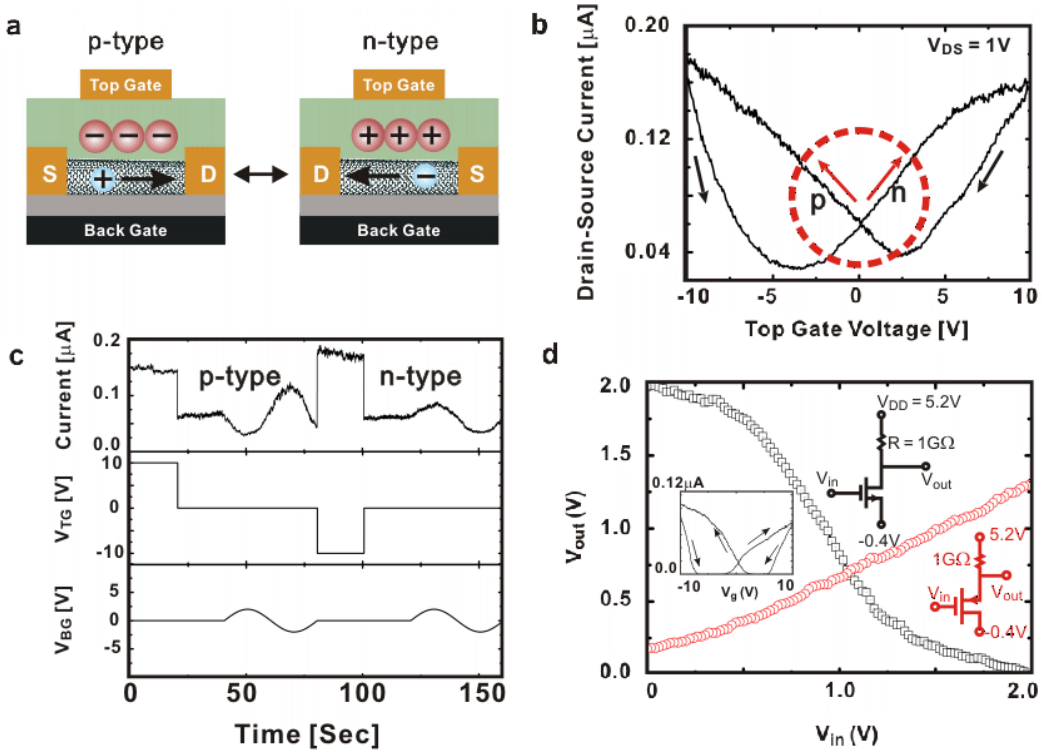

Figure 3. Type-switchable FETs based on CNTs and NPs. (a) Operation of type-switchable transistors. (b) Gating effect of a typical type-switchable FET. The crossing point showing both n- and p-type behaviors is marked by a dotted circle. (c) Real-time switching of swCNT–FET types. After applying a large positive (or negative) top-gate bias, a small back-gate bias was used to confirm the p-type (or n-type) behavior of the channel. (d) Switching the inverter functionality using a type-switchable FET.

an n-type or p-type channel, respectively. Presumably, in the forward sweep, the initial −10 V gate bias charged the NPs positively, resulting in n-type channels (left of figure 3(a)). In a similar way, we can expect p-type characteristics in the reverse sweep (right of figure 3(a)). Note that the hysteresis curve is quite symmetric, which presumably originates from the ambipolar properties and symmetric band structures of swCNTs. We could achieve similar characteristics from most of our devices when a high-quality Al_2O_3 layer was used as a dielectric layer to cover up swCNT surfaces. However, when we used poor leaky dielectric layers (e.g. a SiO_2 layer deposited in a low vacuum chamber), oxygen from the air got bound to the swCNT channel surfaces, and our devices exhibited p-type characteristics with asymmetric hysteresis curves as reported previously [18].

Figure 3(c) shows the type-switching of our FET devices. Here, the charges in NPs were controlled by applying large top-gate voltage, and the gating effect of the channel was measured using a small back-gate bias. First, a large positive top-gate voltage was applied so that NPs were charged negatively. Then, a small sinusoidal bias was applied to the back-gate while monitoring source–drain currents. Note that the current decreased as the back-gate bias increased, indicating a p-type behavior. After a large negative bias to the top-gate, the current increased as the back-gate bias increased, indicating that the channel was switched to n-type. We have ascertained that memory effect in our devices lasted at least for 8000 s. As a matter of fact, the duration of such floating gate-based devices is mainly determined by the quality of gate oxide layers which should be easily improved when the technology is

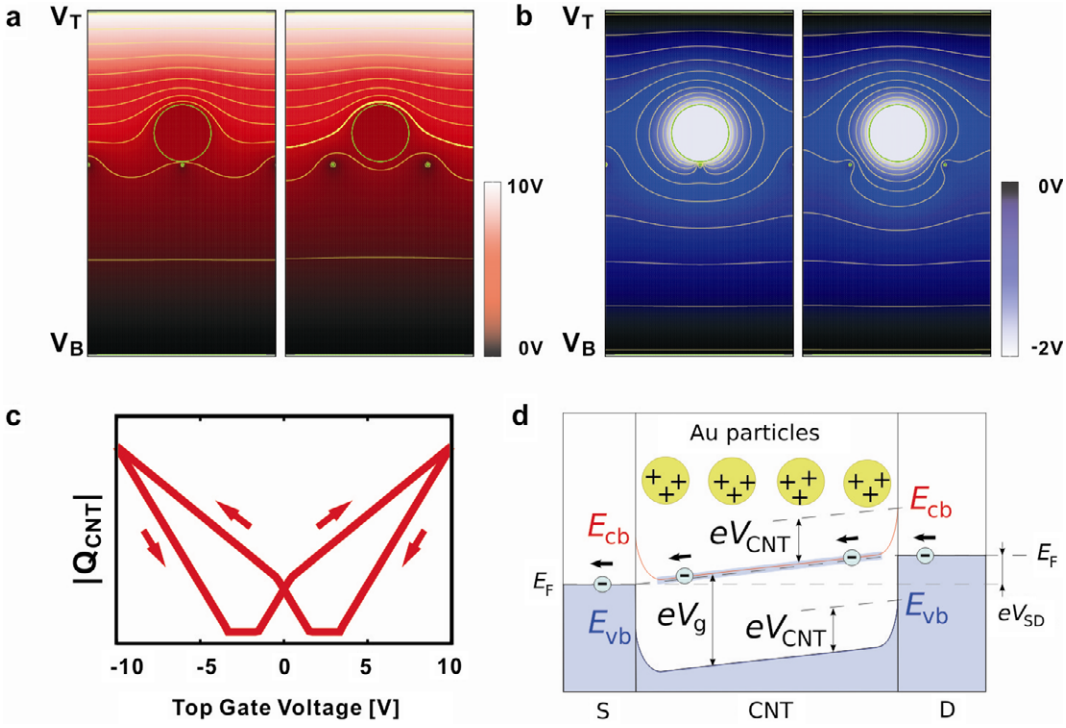

Figure 4. Computational modeling. (a) Electric potential plots with equipotential contour lines at $V_T = 10$ V for two different configurations. The large gray (green) circles and small gray (green) dots represent a 30 nm-diameter Au NP and 1 nm-diameter swCNT, respectively. The gap between the swCNT layer and the Au NP is 1 nm. V_T and V_B are the potentials of top- and bottom-gates, respectively. The swCNTs are connected to the source–drain electrodes. The Au NP and semiconducting swCNTs are saturated to $V_{Au} = 2.0$ V and $V_{CNT} = 0.5$ V, respectively. (b) Electric potential after the top-gate voltage is turned off from $V_T = 10$ V. In this case, $V_{Au} \approx -1.86$ V and $V_{CNT} = -0.5$ V. (c) Absolute values of excess charges of the semiconducting swCNTs as a function of the top-gate voltage. These charges are proportional to the drain–source current shown in figure 2(e). (d) Schematic band diagram along the semiconducting swCNT channel when the potential of the swCNT is held to its saturated value due to Au NPs, and a small source–drain bias voltage is applied. The shaded (blue-colored) region visualizes the filled electric states.

industrialized. A similar experiment could be performed using a single gate (figure S1 in supporting information available at stacks.iop.org/Nano/21/345301/mmedia).

The capability of switching FET types allowed us to reconfigure the functionality of logic gates such as an inverter (figure 3(d)). Here, a load resistor of 1 GΩ was connected between the transistor drain and a 2 V bias (V_{DD}). First, a large negative top-gate bias (−10 V) was applied to charge NPs positively, which switched the swCNT–FET to n-type. Then, the output potential (V_{out}) was measured while sweeping the gate bias (V_{in}). Since the swCNT–FET operated as an n-type FET, the increasing gate bias should reduce the resistance of the swCNT–FETs, resulting in a drop of V_{out} with increasing gate bias V_{in} just like an inverter (empty squares in figure 3(d)). When a large positive top-gate bias was applied (+10 V), NPs were charged negatively, and the swCNT–FET exhibits p-type characteristics. Thus, V_{out} should have the same polarity as V_{in} (empty circles in figure 3(d)). In complicated logic devices, the output voltage signal of one logic gate works as the input of the following one. Thus, the minimum requirement for data transfer in logic devices is that the input and output voltage swings of individual logic gates should be the same. Our devices, when operating as an inverter logic gate, exhibited identical input and output voltage swings of 0–2 V, meeting the requirement of a component of logic devices. The performance of our devices as a logic gate is still poor compared with conventional silicon-based logic gates. However, since there are already many reports about high-performance CNT-based devices [2–4], our device performance should be improved by various future modifications such as quality improvement of CNT materials and nanoparticles and the usage of high-k dielectric materials. More importantly, it should be noted that the major advantage of our devices compared with conventional architectures such as CMOS-based logic gates is the real-time reconfiguration of its logic functionality. Considering that our device fabrication method is scalable from nanoscale to macroscale [21], this result clearly shows the possibility of new practical applications in the future.

3.2. *Theoretical analysis*

We built a theoretical model to analyze the reconfigurable devices (supplementary information available at stacks.iop.org/Nano/21/345301/mmedia). Here, we considered a model system comprised of semiconducting swCNTs, NPs, a top-gate, a bottom gate, and an insulating layer (figures 4(a) and (b)). Two different configurations were considered: (i) the NP was right above one swCNT, while the other swCNT was located at the boundary, and (ii) the NP was in between two neighboring swCNTs. For each configuration, we solved the Laplace equation numerically to determine the coefficients of potential or the coefficients

of capacitance/induction, C_{ij}, which depend only on the geometry of the configuration. The potentials of Au NPs and swCNTs (V_{Au} and V_{CNT}, respectively), and the excess charges Q_{Au} and Q_{CNT} accumulated in them for any given top and bottom gate voltages V_T and V_B, were calculated using

$$Q_{Au} = C_{AT}V_T + C_{AB}V_B + C_{AC}V_{CNT} + C_{AA}V_{Au} \quad (1)$$

$$Q_{CNT} = C_{CT}V_T + C_{CB}V_B + C_{CC}V_{CNT} + C_{CC}V_{Au} \quad (2)$$

C_{ij} were evaluated by taking an average over two different configurations [23].

Here, we assumed that the potential $|V_{CNT} - V_{Au}|$ could not exceed a certain saturated potential V_c due to the tunneling current through the thin oxide between the swCNT and NP at a large bias. V_c was chosen to be 1.5 V based on the breakdown field (0.3–0.5 V nm^{-1}) [24, 25] of the Al_2O_3 layer. On the other hand, for a semiconducting swCNT, its Fermi level can change by a gate bias but only within the electronic band gap; once the Fermi level meets the band edges at large gate bias, electronic self-energy should dominate the total energy preventing further change in the Fermi level [26]. Here, we assumed that V_{CNT} cannot exceed the saturated potential $\pm V_g/2$, where V_g is the potential corresponding to the semiconducting swCNT band gap and is chosen to be 1 V (see supplementary information for voltage saturation available at stacks.iop.org/Nano/21/345301/mmedia).

Figures 4(a) and (b) show gray-scaled (color-coded) electric potentials of our model systems with equipotential contour lines for $V_T = 10$ V and when the top-gate voltage is turned off ($V_T = 0$ V), respectively. Due to the remaining excess charges in NPs, swCNTs experience electric potential even after turning off the top-gate voltage. The simulated hysteresis curves of the potential and excess charges in the NP are presented in figure S2 in supporting information (available at stacks.iop.org/Nano/21/345301/mmedia).

Figure 4(c) shows the calculated excess charges on the semiconducting swCNTs given in absolute values. Due to the high density of states at the lowest conduction (highest valence) band, it is reasonable to state that the excess electrons or holes are all in a degenerate state, contributing to the number of conduction channels. In other words, $|Q_{CNT}|$ should be proportional to the source–drain current. Indeed, it (figure 4(c)) agrees well with the measured I–V_g curve (figure 3(b)). Figure 4(d) shows a schematic band diagram along the semiconducting swCNT channel when its potential is saturated due to the charged NPs, and also shows how the current flows when the bias voltage is applied. Note that there would be no current flow unless the voltage is saturated because the Fermi level would be located in the gap.

4. Conclusion

We developed type-switchable FETs, where the charges stored in NPs adjacent to CNT device channels were utilized to control the carrier type and density in the channels. By this method, we successfully demonstrated the real-time type-switching of swCNT–FETs and inverter logic gates. This result should provide a huge flexibility to the electronics industry.

Acknowledgments

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References

[1] Saito R, Dresselhaus G and Dresselhaus M S 1998 *Physical Properties of Carbon Nanotube* (London: Imperial College Press)
[2] Bachtold A, Hadley P, Nakanishi T and Dekker C 2001 *Science* **294** 1317
[3] Martel R, Schmidt T, Shea H R, Hertel T and Avouris Ph 1998 *Appl. Phys. Lett.* **73** 2447
[4] Dai H, Hafner J H, Rinzler A G, Colbert D T and Smalley R E 1996 *Nature* **384** 147
[5] Freitag M, Chen J, Tersoff J, Tsang J, Fu Q, Liu J and Avouris Ph 2004 *Phys. Rev. Lett.* **93** 076803
[6] Derycke V, Martel R, Appenzeller J and Avouris Ph 2001 *Nano Lett.* **1** 453
[7] Liu X L, Lee C, Zhou C W and Han J 2001 *Appl. Phys. Lett.* **79** 3329
[8] Cui J B, Sordan R, Burghard M and Kern K 2002 *Appl. Phys. Lett.* **81** 3260
[9] Zhou C, Kong J, Yenilmez E and Dai H 2000 *Science* **290** 1552
[10] Kazaoui S, Minami N, Matsuda N, Kataura H and Achiba Y 2001 *Appl. Phys. Lett.* **78** 3433
[11] Tiwari S, Rana F, Hanafi H, Hartstein A, Crabbe E F and Chan K 1996 *Appl. Phys. Lett* **68** 1377
[12] Fuhrer M S, Kim B M, Durkop T and Brintlinger T 2002 *Nano Lett.* **2** 755
[13] Lu X B and Dai J Y 2006 *Appl. Phys. Lett.* **88** 113104
[14] Ganguly U, Kan E C and Zhang Y 2005 *Appl. Phys. Lett.* **87** 043108
[15] Arnold M S, Green A A, Hulvat J F, Stupp S I and Hersam M C 2006 *Nat. Nanotechnol.* **1** 60
[16] Purewal M S, Hong B H, Ravi A, Chandra B, Hone J and Kim P 2007 *Phys. Rev. Lett.* **98** 186808
[17] Nemec N, Tomanek D and Cuniberti G 2006 *Phys. Rev. Lett.* **96** 076802
[18] Lee M, Im J, Lee B Y, Myung S, Kang J, Huang L, Kwon Y-K and Hong S 2006 *Nat. Nanotechnol.* **1** 66
[19] Myung S, Lee M, Kim G, Ha J and Hong S 2005 *Adv. Mater.* **17** 2361
[20] Collins P G, Arnold M S and Avouris Ph 2001 *Science* **292** 706
[21] Lee M, Lee J, Kim T, Lee H, Lee B Y, Park J, Seong M and Hong S 2010 *Nanotechnology* **21** 055504
[22] Lee D U, Lee M S, Kim J, Kim E K, Koo H, Cho W and Kim W M 2007 *Appl. Phys. Lett.* **90** 093514
[23] Jackson J D 1999 *Classical Electrodynamics* 2nd edn (New York: Wiley) chapter 1
[24] Kawakami N, Yokota Y, Tachibana T, Hayashi K and Kobashi K 2005 *Diamond Relat. Mater.* **14** 2015
[25] Groner M D, Fabreguette F H, Elam J W and George S M 2004 *Chem. Mater.* **16** 639
[26] Datta S 1995 *Electronic Transport in Mesoscopic Systems* (Cambridge: Cambridge University Press) pp 7–47