Majority Carrier Type Conversion with Floating Gates in Carbon Nanotube Transistors

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In a conventional silicon transistor, the type of carrier is determined *a priori* by the dopant type. Modern electronic devices have been developed based on these fixed-polarity transistors. However, carbon nanotubes (CNTs) have shown p-type behavior under ambient conditions.[1,2] More interestingly, ambipolarity (in which the majority carrier is determined by the gate voltage) has been observed under vacuum and with a top gate oxide.[3–5] The unique ambipolarity of carbon nanotubes has been regarded as a drawback in their application to Si technology. To suppress the ambipolarity of the CNTs in CNT-based complementary metal oxide semiconductor (CMOS) technology, numerous chemical dopants such as amine-rich polymers, alkali metals, and nitronium ions, and various doping methods[6–16] have been suggested to control the majority carrier type of CNTs. The multiple gate structure has also been suggested for controlling1 the majority carrier type of CNTs but this function disappears when the voltage is not applied.[4]

On the other hand, the charge trap layer in a top-floating gate device in conventional semiconductor technology has been used to fabricate nonvolatile memory devices. CNTs have also been used for the fabrication of nonvolatile memory devices that utilize the charge trap layer.[17–27] In this study, the charge trap layer in a top-floating gate was used to determine the majority carrier type of the CNT channel. Additionally, carrier-type controlled inverters were fabricated. We demonstrated that single and multilevel nonvolatile memory devices can be operated with a controllable majority carrier type. This freedom is an additional function compared to Si devices, and could open up new opportunities in designing CNT-based nanodevices for terabit integration.

Figure 1a shows a schematic of a nonvolatile memory cell. Charges can be trapped in the trap layer through the thin tunneling oxide by the control gate. A thick layer of blocking gate was implemented to prevent charge sloshing from the control gate. The channel between the source and drain consists of randomly networked single-walled (SW)CNTs synthesized by plasma-enhanced chemical vapor deposition (PECVD; Fig. 1b and c). This device clearly showed ambipolarcurrent–gate voltage (I–V_G) characteristics over a large V_G range (Fig. 1d), having hole carriers at a negative gate bias and electron carriers at a positive gate bias. Large hysteresis was also observed due to the presence of the trap layer. The large hysteresis and ambipolarity of the CNT-transistor provide the ability to design programmable logic circuits and memory cells.

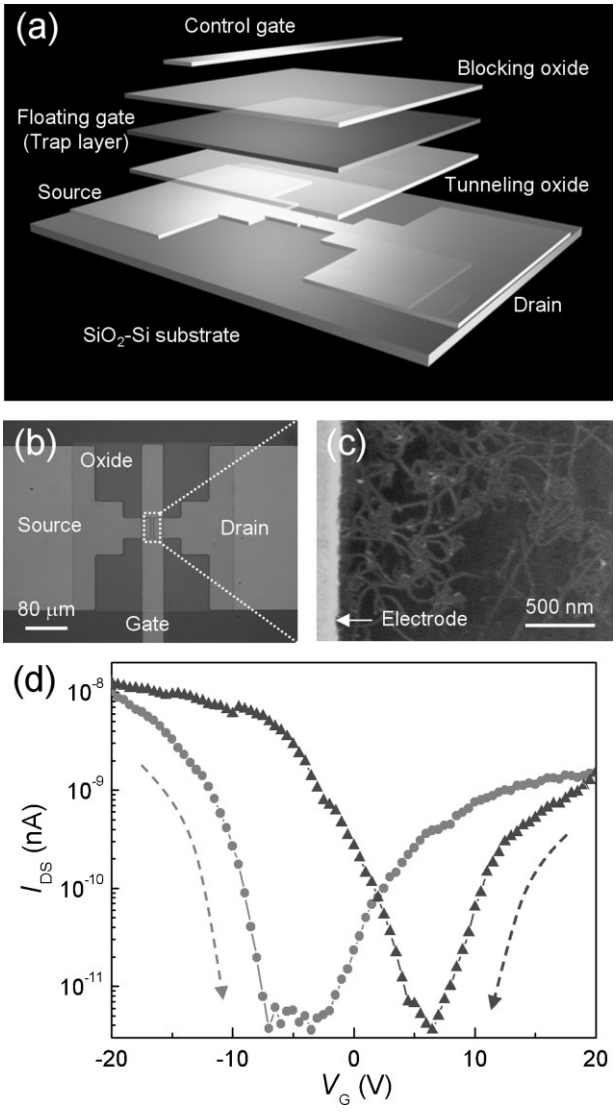

Figure 1. a) Three dimensional schematic of the CNT transistor with a floating gate and control top-gate. b) Optical microscopy image of a thin film transistor (top view). c) The morphology of a random network CNT in the channel area grown directly by PECVD. d) I–V_G characteristics of CNT-TFTs demonstrating large hysteresis with voltage sweeping induced by trapped charges in the floating gate.

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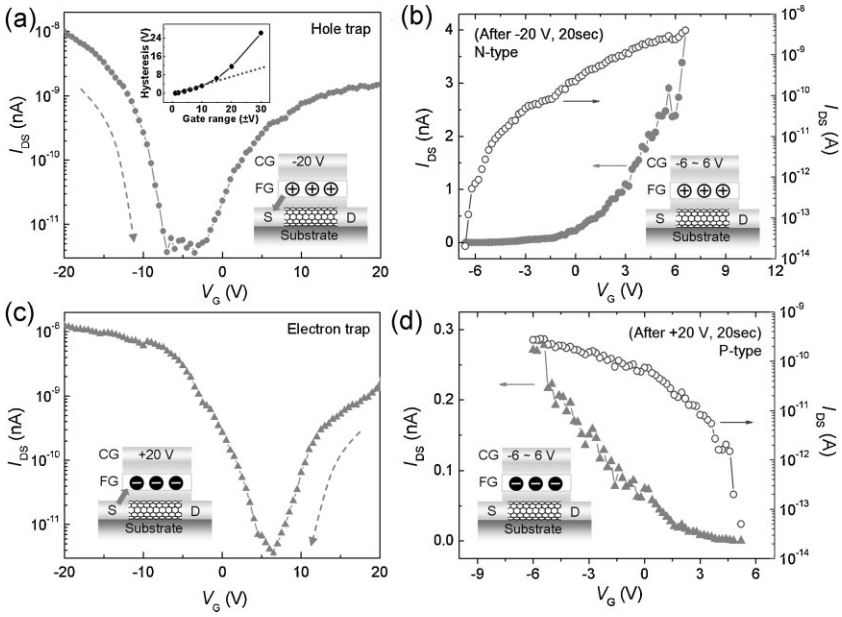

Figure 2. Procedure for charge trapping and the corresponding I–V_G characteristics. a) Holes were trapped in the trap layer when the voltage was swept from −20 to 20 V, and b) I–V_G characteristics after charging holes in the trap layer by applying a control gate bias at −20 V for 10 s. c) Electrons were trapped in the trap layer when voltage was swept from +20 to −20 V, and d) I–V_G characteristics after charging electrons in the trap layer by applying a control gate bias at +20 V for 10 s.

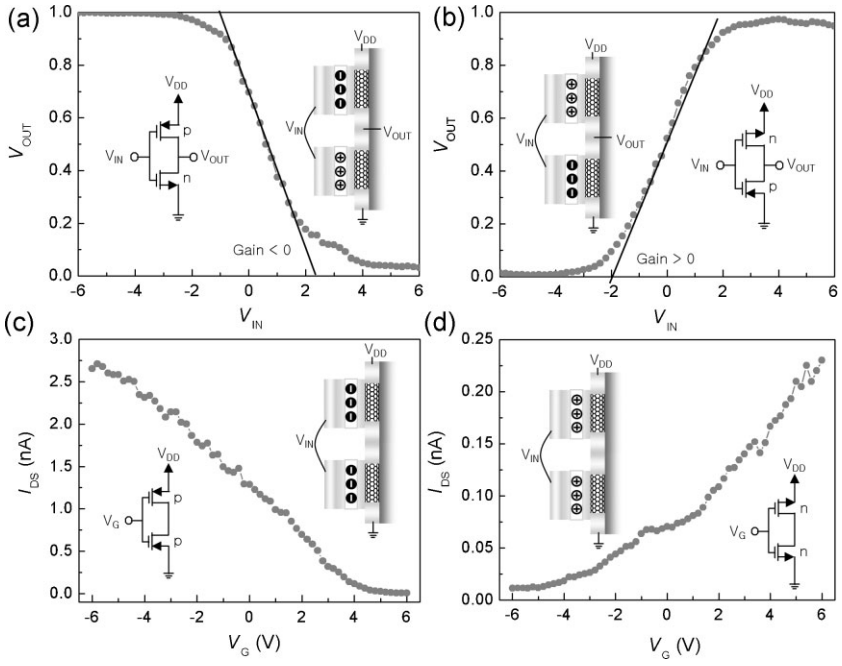

Figure 3. Convertible inverters with two transistors in various trapped charges. Four different types of inverter depending on the trapped charges: a) p-type transistor near V_{DD}, and n-type transistor near ground, b) n-type transistor near V_{DD}, and p-type transistor near ground, c) both p-type transistors, and d) both n-type transistors.

Hysteresis is typically observed in CNT transistors even without a trap layer when a back gate is present. This is attributed to the presence of ambient gases on the CNTs or between the CNTs and the gate oxide.[28–32] For low gate biases (<10 V) at which tunneling charges did not accumulate in the trap layer, hysteresis existed due to the presence of trap states at the interface between the CNTs and the tunneling oxide, as shown in the inset of Figure 2a. At a high gate bias (>10 V), the hysteresis increased exponentially with gate bias due to the charges accumulated in the trap layer. The exponential increase of hysteresis is evidence for the existence of a tunneling current through the oxide layer, where the tunneling probability is proportional to $e^{-2\sqrt{(2m*/\hbar^2)(E_{Pb}-E)}-L}$. Here, m^* is the effective mass of the electron, $\hbar$ is Planck's constant, E_{Pb} is the barrier height of the oxide layer, E is the gate potential, and L is the thickness of the oxide layer.[33] Therefore, in our case, it was necessary to use a large gate bias (>10 V) to trap charges in the trap layer by tunneling.

When the gate bias was swept from −20 V to +20 V, holes were trapped in the trap layer at −20 V, causing the threshold voltage to decrease (Fig. 2a). To trap holes in the trap layer, −20 V was applied for 20 s (Fig. 2b). As a consequence, the channel showed n-type behavior in the gate bias range from −6 V to + 6 V. Because there was no charge tunneling in this gate range, the n- or p-type characteristics were retained (inset of Fig. 2a). The electron trap was created in an analogous manner (Fig. 2c). When the gate bias was swept from +20 V to −20 V, electrons were trapped in the trap layer at +20 V, increasing the threshold voltage. Thus, +20 V was applied for 20 s to accumulate electrons in the trap layer. This resulted in a p-type transistor, as shown in Figure 2d. This demonstrates that the majority carrier can be altered by the polarity of the trapped charges in the trap layer, i.e., a floating FET is created using the trap layer. The idea of a trap layer exists in Si technology, but the type conversion of the channel is an additional function of the ambipolar CNT-transistor that could be beneficial in future applications.

To confirm the type conversion of the transistors, an inverter was fabricated using two CNT-FETs. A p-type transistor using an electron trap near the supply voltage (V_{DD}), and an n-type transistor using a hole trap near ground generated typical inverter characteristics for V_{OUT} (0 and 1) with V_{IN} variables (Fig. 3a). In this case, a positive gain was

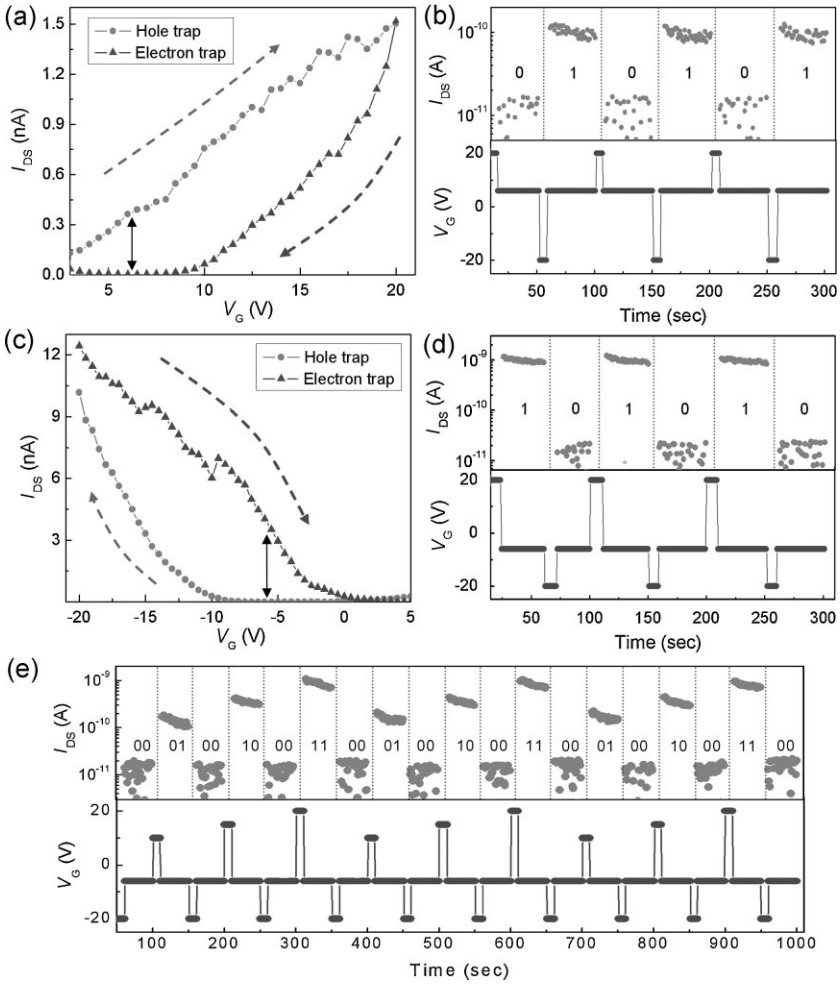

Figure 4. Convertible nonvolatile memory cell: a) Hysteresis curve caused by trapped charges (hole trap in top red-circle curve and electron trap in bottom green-triangle curve), and b) the corresponding (0,1) series of 1-bit cells. The majority carrier type was electrons. Data in c) and d) are analogous to (a) and (b) but the majority carrier type was holes. e) A 2-bit multilevel cell controlled by the amount of trapped charges, i.e., by the applied voltages.

obtained. On the other hand, with an n-type transistor near V_{DD} and p-type transistor near ground (i.e., with type conversion), similar inverter characteristics were obtained but with positive gain polarity (Fig. 3b). In the inverter using two electron-trapped transistors, simple p-type behavior was obtained, as shown in Figure 3c. Similarly, n-type behavior was obtained using two hole-trapped transistors (Fig. 3d). We emphasize here that the inverter type can be easily converted by changing the polarity of the trapped charges in the trap layer. A convertible inverter cannot be realized in Si technology, since the majority carrier type is fixed.

We also demonstrated a convertible nonvolatile memory device using this top-floating gate CNT-FET. When electrons were trapped in the trap layer at a gate bias of +20 V, the threshold voltage increased, as previously mentioned (Fig. 2c). In this case, the drain current (I_{DS}) at 6 V was nearly zero (Fig. 4a). When holes were trapped at a gate bias of −20 V, the threshold voltage decreased and I_{DS} at a read voltage of 6 V was high. At a gate bias of +6 V, the majority carriers in the CNT channel were electrons, thus the (0,1) 1-bit was repeated, as shown in Figure 4b. If the memory bit was operated at a read voltage of −6 V, the (1,0) 1-bit was repeated in reverse (Fig. 4c and d). The majority carriers were holes in this case. The (0,1) or (1,0) 1-bit together with the majority carrier type could be controlled by the polarity of the trapped charges. A 2-bit multilevel nonvolatile memory cell could also be constructed, as shown in Figure 4e. At a gate bias of −20 V, holes were trapped, and no current flowed at −6 V. At a gate bias of 10 V, a hole current flowed at −6 V. With increasing gate bias, the hole current also increased at −6 V. The current magnitudes at gate biases of 10, 15, and 20 V were clearly distinguished from each other. This was repeatable with many cycles. Thus, 2-bit memory was demonstrated with hole carriers.

In summary, type conversion of the CNT channel was realized by controlling the charge polarity in the top trap layer. Although the idea of a trap layer exists in Si technology, the operation of a CNT transistor provided more freedom in determining the majority carrier of the channel. We were able to demonstrate a convertible inverter, that gain polarity could be changed, and a nonvolatile memory device using the floating CNT-FET. This offers possibilities for designing CNT based CMOS logic circuits.

Experimental

An array of thin film transistors (TFTs) was fabricated with randomly networked SWCNTs that were selectively synthesized on an array of catalyst photoresists (0.01 M of ferrocene) [34] using remote plasma-enhanced chemical vapor deposition (PECVD) at a low temperature (450 °C) [35]. The corresponding source and drain electrodes composed of Ti (5 nm)/Au (50 nm) (channel lengths: 2, 3, 5, 7, 10 μm; width: 40 μm, 20 channels for each length in the sample) were deposited to form an array of 200 TFTs. A thin film of top-gate tunneling oxide (Al_2O_3, 5 nm)-metal trap layer (7 nm)-blocking oxide (Al_2O_3, 50 nm) was deposited by atomic layer deposition at 150 °C. The gate electrode (Ti (5 nm)/Au (50 nm)) was formed similarly to the source and drain electrodes. The yield of transistors with on/off ratio of greater than 10^4 was 88% [5]. The detailed method has been described elsewhere [34,35]. Logic circuits were fabricated by connecting several TFTs with gold wire using wire bonder. The *I–V* characteristics of the CNT-TFTs were measured under ambient conditions by a source-measure unit (Keithley 236, 237) using a probe station. Scanning electron microscope (JEOL, JSM-7401F) images were taken in secondary electron image mode under a pressure of $\sim 4 \times 10^{-3}$ Torr (1 Torr ~ 133.3 Pa).

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